REMARKS

The claims have been amended in view of the Office action and in view of the remarks which follow, they are believed to be in condition for allowance.

Non Compliant Claim Objections

In section 1 of the detailed action, several claims were objected on the grounds of being non-compliant. It is believed that those grounds of rejection have been overcome. Accordingly, that issue is believed to be moot.

Claim Objections

In section 3 of the detailed action, claim 25 was found objectionable. As claim 25 has been canceled, that issue is believed to be moot.

Specification

Because the specification was found to be confusing and needed correction of grammatical errors, many changes have been made but no new matter has been added. The names of elements in the drawings having the same reference indicia are now believed to be consistent in view of the amendments pertaining thereto.

Replacement Drawings

Replacement drawings have been filed contemporaneously herewith to comply with the rules and to add labels drawn from the text to make the drawings more easily understood

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Claim Rejections - 35 USC § 103

In section 4 of the detailed action, claims 1, 4, 8-13, 19-28, 30, 31, 34, 38-40, and 46-50 were rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al. U.S. Patent No. 6,425,075 (Stiles) in view of Cummins U.S. Patent No. 6,263,427 (Cummins)

With reference to section 4 of the detailed action pertaining to claim 1, the Office Action cites FIG. 2 and text in Cols. 9 and 10 where Stiles teaches a method of operating a computer having a pipelined processor having "First Level Branch Prediction Cache 152" and "Second Level Branch Prediction Cache 155" which were alleged to be Branch Target Buffers (BTB's). The "First Level Branch Prediction Cache 152" is shown in detail in FIG. 3 and described at Col. 10,lines 37-40 as containing a Least Recently Used (LRU) logic block 181 which selects a BPC line to be overweriten by a new block of instruction data, which clearly is not a LIFO (Last In First Out) function.

Applicants respectfully submit that an LRU does not suggest a FIFO. A FIFO is "First In - First Out" device. When an LRU (Least Recently Used) algorithm is used,a new entry is to be entered in a set-associative array (storage device), it determines which entry is to be replaced. These two structures differ for FIFO replaces the oldest entry in the queue/storage device (the oldest is the first entry placed into the queue/storage device). With respect to LRU, the oldest entry could have been the last entry referenced. In such a case, it would be the MRU (Most Recently Used). As such, some other entry, the LRU, entry which is not the oldest entry, would be replaced. Accordingly, it is respectfully submitted that what Stiles teaches is divergent from the subject matter of the three amended independent claims in the instant application and teaches away therefrom with regard to the FIFO feature.

In section 6 of the detailed action, the Office Action admits that Stiles fails to disclose delaying the pipeline until a branch prediction unit finishes the prediction, but it is alleged that Cummins discloses what Stiles lacks referring to col 8 lines 32-42 thereof opining that Stiles would have been motivated to emulate Fig. 7 of Cummins to reduce hardware, processor area, and complexity of correcting the delay. However, stalling the processor is not what is claimed by the amended claims herein since the specification calls for delaying the decoding of a branch, not stalling of the processor. Thus the claims have been corrected to call for delaying of decoding, not stalling the processor. In accordance with this invention, the pipeline is delayed by by blocking redundant data, but the processor is not stalled. Accordingly, Cummins is believed not to be relevant to the amended claims.

In section 7 of the detailed action it is stated as follows:

> "Stiles fails to disclose it comprising blocking an entry matching an entry within the recent entry queue from being written into the BTB and that the BTB and recent entry queue are set associative."
>
> "Official Notice is taken that arranging the caches in a tiered arrangement (like a typical L1 -L2 cache setup) is well known in the art. A tiered arrangement of cache levels allows the system to write an entry into only the L1 cache rather than spending the time and resources to write into both the L1 and L2. Upon eviction from the L1 cache, the entry is written into the L2. The examiner asserts that with this arrangement, any entry (including those that match current entries in the LI) will be blocked from writing to the L2 cache.
>
> "Official Notice is taken that the recent entry queue (and therefore, BTB) can use set associative rather than direct mapped. Stiles would have been motivated to utilize this change if he desired to alter the size of the recent entry queue. Then a set associative technique would be the preferred technique."
>
> "It would have been obvious to one of ordinary skill in the art at the time of invention to have arranged Stiles' caches in a tiered L1-L2 arrangement for the benefit of conserving system resources on writing an entry to the BTB.

It is respectfully submitted that the function of an L1-L2 cache setup does not perform the function of comparing entries being made to the BTB in parallel with the recent entry queue to avoid redundant entries into the BTB. That is not the way that L1 and L2 caches setups operate. Thus, it is believed that thee official notice allegation cannot be sustained. It is submitted that a BTB is different from an instruction/data cache. In an instruction/data cache, access is being made to a particular/precise address. In a BTB, a starting address is provided and the **closest** branch to that address is reported. As such, a BTB does not work with the same principles as that of a data/instruction cache. As such, there are short falls to not having the 1st level branch table be a subset of the 2nd level branch table as suggested in section 7 of the Office Action. It is respectfully submitted that tThe case defined by IBM where the 1st level table does predictions is only in the case of detected loops where the known prediction from the 1st level table will be the same as that from the second level table. In all cases where a loop is not involved, it can not be guaranteed that the prediction from the 1st and 2nd level tables can be the same.

It is not possible to respond to the portion of the Office Action which trailed off as follows: "It further would have been obvious to allow...."

The statements in sections 8–27 of the detailed action are believed to be moot in view of the amendments to the claims and the above remarks.

In view of the amendments and the above remarks, the claims and the application as a whole are now believed to be patentable over the prior art of record.

No fee is believed to be due for the submission of this amendment. If any fees are required, however, please charge such fees to Deposit Account No. 09-0463.

In view of the amendments and the above remarks favorable action including allowance of the claims and the application as a whole are respectfully solicited.

Respectfully submitted,

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